

5 loading, at the tester, the kernel test patterns stored in the tester memory onto an on-board
6 memory of a complex device under test (DUT);

7 executing, at the complex device under test (DUT), a re-generative functional test of the
8 complex device under test (DUT) by applying the kernel test patterns to the complex device
9 under test (DUT); and

10 comparing, at the tester, a test result of the re-generative functional test with an expected
11 test result to check for manufacturing defects.

1 2. (Amended) The method as claimed in claim 1, wherein said FRIT kernel includes a
2 software built-in self-test engine (SBE) to execute the re-generative functional test of the
3 complex device under test (DUT), and the expected test result obtained from computer modeling
4 of the complex device under test (DUT).

1 4. (Amended) The method as claimed in claim 2, wherein said software built-in self-test
2 engine (SBE) of the FRIT kernel comprises:

3 a RIT generator including compact RIT machine code reside in the on-board memory of
4 the complex device under test (DUT) for generating the re-generated functional test;

5 a test program execution module including test execution directives for providing an
6 environment to store and run the re-generated functional test; and

7 a test result compaction module including compression machine code to compress test
8 results of the re-generated functional test for storage in the on-board memory of the complex
9 device under test (DUT).

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1 6. (Amended) The method as claimed in claim 1, wherein said complex device under test
2 (DUT) includes a microprocessor.

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1 8. (Amended) The method as claimed in claim 7, wherein said FRIT kernel includes a
2 software built-in self-test engine (SBE) to execute the re-generative functional test of the
3 complex device under test (DUT), and the expected test result obtained either from computer
4 modeling of the complex device under test (DUT) or from a known good device.

1 11. (Amended) A computer readable medium having stored thereon a functional
2 random instruction test (FRIT) kernel which, when executed by a system, cause the system to
3 perform:

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4 receiving the FRIT kernel in kernel test patterns and storing the kernel test patterns in a
5 tester memory;

6 loading the kernel test patterns stored in the tester memory onto an on-board memory of
7 a complex device under test (DUT);

8 enabling execution, at the complex device under test (DUT), a re-generative functional
9 test of the complex device under test (DUT) by applying the kernel test patterns to the complex
10 device under test (DUT); and

11 making a comparison between a test result of the re-generative functional test and an
12 expected test result to check for manufacturing defects.

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12. (Amended)

The computer readable medium as claimed in claim 11, wherein
said FRIT kernel includes a software built-in self-test engine (SBE) to execute the re-generative
functional test of the complex device under test (DUT), and the expected test result.

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14. (Amended)

The computer readable medium as claimed in claim 12, wherein
said software built-in self-test engine (SBE) of the FRIT kernel comprises:

a RIT generator including compact RIT machine code in the on-board memory of the
complex device under test (DUT) for generating the re-generated functional test;

a test program execution module including test execution directives for providing an
environment to store and run the re-generated functional test; and

a test result compaction module including compression machine code to compress test
results of the re-generated functional test for storage in the on-board memory of the complex
device under test (DUT).

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16. (Amended)

The computer readable medium as claimed in claim 11, wherein
said complex device under test (DUT) includes a microprocessor.

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18. (Amended)

The computer readable medium as claimed in claim 17, wherein
said FRIT kernel includes a software built-in self-test engine (SBE) to execute the re-generative
functional test of the complex device under test (DUT), and the expected test result obtained
from computer modeling of the complex device under test (DUT) or from a known good device.

21. (Amended)

A test system for testing a complex device, comprising:

2 a complex device under test (DUT) having an on-board memory; and
3 a tester including a tester memory to test a functionality of the complex device under test
4 (DUT) by:
5 receiving the FRIT kernel in kernel test patterns and storing the kernel test
6 patterns in the tester memory;
7 loading the kernel test patterns stored in the tester memory onto the on-board
8 memory of the complex device under test (DUT);
9 enabling execution, at the complex device under test (DUT), a re-generative
10 functional test of the complex device under test (DUT) by applying the kernel test
11 patterns to the complex device under test (DUT); and
12 making a comparison between a test result of the re-generative functional test and
13 an expected test result to check for manufacturing defects.

1 **22. (Amended)** The test system as claimed in claim 21, wherein said FRIT kernel
2 includes a software built-in self-test engine (SBE) to execute the re-generative functional test
3 of the complex device under test (DUT), and the expected test result.

1 **24.** The test system as claimed in claim 22, wherein said software built-in self-test
2 engine (SBE) of the FRIT kernel comprises:
3 a RIT generator including compact RIT machine code in the on-board memory of the
4 complex device under test (DUT) for generating the re-generated functional test;
5 a test program execution module including test execution directives for providing an
6 environment to store and run the re-generated functional test; and

a¹⁰₈ a test result compaction module including compression machine code to compress test
results of the re-generated functional test for storage in the on-board memory of the complex
9 device under test (DUT).

a¹¹₂ 26. (Amended) The test system as claimed in claim 21, wherein said complex
device under test (DUT) includes a microprocessor.

a¹²₃ 28. (Amended) The test system as claimed in claim 27, wherein said FRIT kernel
includes a software built-in self-test engine (SBE) to execute the re-generative functional test
of the complex device under test (DUT), and the expected test result obtained from computer
4 modeling of the complex device under test (DUT) or from a known good device.

a¹³₃ --31. A complex device, comprising:
a memory to store a functional random instruction testing (FRIT) kernel in kernel test
patterns; and
4 a processor to perform a re-generative functional test of the complex device under test
5 (DUT) upon execution of the kernel test patterns and to enable comparison between a test result
6 of the re-generative functional test and an expected test result to check for manufacturing
7 defects.

1 32. The complex device as claimed in claim 31, wherein said FRIT kernel includes
2 a software built-in self-test engine (SBE) to execute the re-generative functional test of the
3 complex device under test (DUT), and the expected test result.

1 33. The complex device as claimed in claim 32, wherein said expected test result is
2 obtained from computer modeling of the complex device under test (DUT) or from a known
3 good device.

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34. The complex device as claimed in claim 32, wherein said software built-in self-
test engine (SBE) of the FRIT kernel comprises:

 a RIT generator including compact RIT machine code to reside in the on-board memory
4 of the complex device under test (DUT) for generating the re-generated functional test;

5 a test program execution module including test execution directives for providing an
6 environment to store and run the re-generated functional test; and

7 a test result compaction module including compression machine code to compress test
8 results of the re-generated functional test for storage in the on-board memory of the complex
9 device under test (DUT).

1 35. The complex device as claimed in claim 32, wherein said test execution
2 environment employs an exception handler for handling illegal conditions such as undesirable
3 memory accesses, deadlock, shut-down, and infinite loops.

1 36. The complex device as claimed in claim 32, wherein, when the kernel test
2 patterns are applied to the processor from the memory, the processor performs the following:
3 beginning a set-up for executing the kernel test patterns;

4 executing the kernel test patterns to generate a series of test sequences and associated
5 data for respective test sequences;
6 running the test sequences, and at the end of the test sequences, obtaining the test results
7 for storage in the on-board memory; and
8 dumping the test results of the kernel test patterns to the tester, via an interface, for
9 enabling said comparison with the expected test result to check for manufacturing defects.

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37. The complex device as claimed in claim 32, wherein said software built-in self-
2 test engine (SBE) of the FRIT kernel is programmed to generate and execute one or more ("N")
3 instruction sequences, each sequence being executed on one or more (M) data sets where N and
4 M represent an integer no less than "1" and are user-specified numbers used in generating the
5 FRIT kernel by an especially designed software tool.

1 38. The complex device as claimed in claim 37, wherein said software built-in self-
2 test engine (SBE) of the FRIT kernel is further programmed to generate one or more signatures
3 to provide a unique identification of the test result of each test sequence and indicate whether
4 the test result of a particular test sequence is "good" or "bad".--
